Literaturverzeichnis

[ACH97] C. J. Alpert, T. Chan, D. J.-H. Huang, I. Markov, K. Yan, "Quadratic Placement Revisited", Proc. of the 34th ACM/IEEE Design Automation Conference DAC, pp. 752-757, 1997

[AHK97] C. J. Alpert, J.-H. Huang, A. B. Kahng, "Multilevel Circuit Partitioning", Proc. of the 34th ACM/IEEE Design Automation Conference DAC, pp. 530-533, 1997

[All90] J. Allen, "Performance-Directed Synthesis of VLSI Systems", Proc. of the IEEE, Vol. 78, No. 2, pp. 336-355, February 1990

[AlK95] C. J. Alpert, A. B. Kahng, "Recent Directions in Netlist Partitioning", Integration, The VLSI Journal, 19 (1-2), pp. 1-81, 1995

[Alp96] C. J. Alpert, "Multi-way Graph and Hypergraph Partitioning", Ph.-D. Thesis, University of California, Los Angeles, 1996

[Anh89] J. Anhalt, "Globale Verdrahtung im PLAYOUT Chip Planner", Diplomarbeit, Fachbereich Informatik, Universität Kaiserslautern, 1989

[ASZ93] J. Altmeyer, B. Schürmann, G. Zimmermann, "Three Phase Chip Planning - Strategy and Flow Control", SFB-124, Report-No. 21/93, Universität Kaiserslautern, Fachbereich Informatik, 1993

[ASZ92] J. Altmeyer, B. Schürmann, G. Zimmermann, "Three Phase Chip Planning - An Improved Top-Down Chip Planning Strategy", International Conference on Computer-Aided Design ICCAD 92, pp. 598-605, 1992

[BKM95] K. D. Boese, A. B. Kahng, B. A. McCoy, G. Robins, "Near-Optimal Critical Sink Routing Tree Constructions", IEEE Transactions on Computer-Aided Design, Vol. 14, No. 12, pp. 1417-1436, December 1995

[BKM94] K. D. Boese, A. B. Kahng, B. A. McCoy, G. Robins, "Rectilinear Steiner Trees with Minimum Elmore Delay", Proc. of the 31st ACM/IEEE Design Automation Conference DAC, pp. 381-386, 1994

[BKR93] K. D. Boese, A. B. Kahng, G. Robins, "High-Performance Routing Trees with Identified Critical Sinks", Proc. of the 30th ACM/IEEE Design Automation Conference DAC, pp. 182-187, 1993

[Boh98] M. Bohr, "Silicon Trends and Limits for Advanced Microprocessors", Communications of the ACM, Vol. 41, No. 3, pp. 80-87, March 1998

[Bre77] M. A. Breuer, "A Class of Min-Cut Placement Algorithms", Proc. of the 14th ACM/IEEE Design Automation Conference DAC, pp. 284-290, 1977

[BuH93] M. Burger, W. Hebgen, "Netzlängenbasierte Partitionierung hierarchischer Strukturentwürfe in der Repartitionierungsphase", SFB-124, Report-No. 43/93, Universität Kaiserslautern, Fachbereich Informatik, 1993

[BuY85]   M. Burstein, M. N. Youssef, "Timing-Influenced Layout Design", Proc. of the 22nd ACM/IEEE Design Automation Conference DAC, pp. 124-130, 1985

[Che83]   N.-P. Chen, "New Algorithms for Steiner Tree On Graphs", Proc. of the Int. Symposium on Circuits and Systems, pp. 1217-1219, 1983

[CHH92]   T.-H. Chao, J.-M. Ho, Y.-C. Hsu, "Zero Skew Net Routing", Proc. of the 29th ACM/IEEE Design Automation Conference DAC, pp. 518-523, 1992

[ChK84]   C. K. Cheng, E. S. Kuh, "Module Placement based on Resistive Network Optimization", IEEE Transactions on Computer-Aided Design, Vol. CAD-3, No 3, pp. 218-225, March 1984

[ChW96]   Y. P. Chen, D. F. Wong, "An Algorithm for Zero-Skew Clock Tree Routing with Buffer Insertion", ED&TC, 1996

[ChW91]   C. K. Cheng, Y. C. A. Wei, "An Improved Two-Way Partitioning Algorithm with Stable Performance", IEEE Transactions on Computer-Aided Design, Vol. 10, No. 12, pp. 1502-1511, December 1991

[CKK95]   J. Cong, A. B. Kahng, C.-K. Koh, C.-W. A. Tsao, "Bounded-Skew Clock and Steiner Routing under Elmore Delay", Proc. of the Int. Conference On Computer-Aided Design ICCAD 95, pp. 66-71, 1995

[CKR92]   J. Cong, A. B. Kahng, G. Robins, M. Sarrafzadeh, C. K. Wong, "Provably Good Performance-Driven Global Routing", IEEE Transactions on Computer-Aided Design, Vol. 11, No. 6, pp. 739-752, June 1992

[CoL95]   J. J. Cong, K. S. Leung, "Optimal Wiresizing under Elmore Delay Model", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 14, No. 3, pp. 321-336, March 1995

[Con91]   J. Cong, "Pin Assignment with Global Routing for General Cell Design", IEEE Transactions on Computer-Aided Design, Vol. CAD-10, No. 11, pp. 1401-1412, November 1991

[CoP86]   J. P. Cohoon, W. D. Paris, "Genetic Placement", Proc. of the International Conference on Computer-Aided Design ICCAD 86, pp. 422-425, 1986

[DAD84]   A. E. Dunlop, V. D. Agrawal, D. N. Deutsch, M. F. Jukl, P. Kozak, M. Wiesel, "Chip Layout Optimization Using Critical Path Weighting", Proc. of the 21st ACM/IEEE Design Automation Conference DAC, pp. 133-136, 1984

[DaK87]   W. Dai, E. S. Kuh, "Simultaneous Floorplanning and Global Routing for Hierarchical Building Block Layout", IEEE Transactions on Computer-Aided Design, Vol. CAD-6, No 5, pp. 828-837, May 1987

[DEK89]   W. W.-M. Dai, B. Eschermann, E. S. Kuh, M. Pedram, "Hierarchical Placement and Floorplanning in BEAR", IEEE Transactions on Computer-Aided Design, Vol. 8, No. 12, pp. 1335-1349, December 1989

[Dij59]   E. Dijkstra, "A Note on Two Problems in Connection with Graphs", Numerische Mathematik, Vol. 1, pp. 269-271, 1959

[DNA90]   W. E. Donath, R. J. Norman, B. K. Agraval, S. E. Bello, S. Y. Han, J. M. Kurtz-
            berg, P. Lowy, R. I. McMillan, "Timing Driven Placement Using Complete Path
            Delays", Proc. of the 27th ACM/IEEE Design Automation Conference DAC, pp.
            84-89, 1990

[DuD96]   S. Dutt, W. Deng, "A Probability-Based Approach to VLSI Circuit Partitioning",
            Proc. of the 33rd ACM/IEEE Design Automation Conference DAC, pp. 100-105,
            1996

[DuK85]   A. E. Dunlop, B. W. Kernighan, "A Procedure for Placement of Standard-Cell
            VLSI Circuits", IEEE Transactions on Computer-Aided Design, Vol. CAD-4, No
            1, pp. 92-98, January 1985

[Eda94]   M. Edahiro, "An Efficient Zero-Skew Routing Algorithm", Proc. of the 31st
            ACM/IEEE Design Automation Conference DAC, pp. 375-380, 1994

[EiJ98]   H. Eisenmann, F. M. Johannes, "Generic Global Placement and Floorplanning",
            Proc. of the 35th ACM/IEEE Design Automation Conference DAC, pp. 269-274,
            1998

[Elm48]   W. C. Elmore, "The Transient Response of Damped Linear Networks with Parti-
            cular Regard to Wide-Band Amplifiers", Journal of Applied Physics, Vol. 19, No.
            1, pp. 55-63, January 1948

[EsK96]   H. Esbensen, E. S. Kuh, "EXPLORER: An Interactive Floorplanner for Design
            Space Exploration", Proc. of the EURO-DAC-96, pp. 356-361, 1996

[FiM82]   C. M. Fiduccia, R. M. Matheyses, "A Linear-Time Heuristic for Improved Net-
            work Partitions", Proc. of the 19th ACM/IEEE Design Automation Conference
            DAC, pp. 175-181, 1982

[Fri98]   G. Frick, "Performance-driven Global Routing im hierarchischen VLSI-Ent-
            wurf", Diplomarbeit, Fachbereich Informatik, Universität Kaiserslautern, 1998

[Fri96]   G. Frick, "Plazierung mit einem verbesserten Inplace-Partitionierungsverfahren
            im Chip Planner des PLAYOUT-Systems", Projektarbeit, Fachbereich Informa-
            tik, Universität Kaiserslautern, 1996

[Gla92]   K. Glasmacher, "Chip Assembly in einem Top-Down VLSI-Entwurfssystem und
            ein Modell zur konkurrenten Layout-Synthese", Dissertation, Universität Kai-
            serslautern, Fachbereich Informatik, 1992

[HaK92]   L. Hagen, A. B. Kahng, "New Spectral Methods for Ratio Cut Partitioning and
            Clustering", IEEE Transactions on Computer-Aided Design, Vol. 11, No. 9, pp.
            1074-1085, September 1992

[Hal70]   K. M. Hall, "An r-dimensional Quadratic Placement Algorithm", Management
            Science, No. 17, pp. 219-229, 1970

[Han66]   M. Hanan, "On Steiner's Problem with Rectilinear Distance", SIAM Journal of
            Applied Mathematics, Vol. 14, No. 2, pp. 255-265, 1966

[Heb95]   W. Hebgen, "Netzlängenbasierte Abschätzung des Zeitverhaltens in einem top-down VLSI-Entwurfssystem", Dissertation, Universität Kaiserslautern, Fachbereich Informatik, 1995

[Hes99]   A. Heß, "Abschätzungstoleranzen im hierarchischen VLSI-Entwurf", Dissertation, Universität Kaiserslautern, Fachbereich Informatik, 1999

[HNY87]   P. S. Hauge, R. Nair, E. J. Yoffa, "Circuit Placement for Predictable Performance", Proc. of the International Conference On Computer-Aided Design ICCAD 87, pp. 88-91, 1987

[HNZ93]   W. Hebgen, P. Nuhn, G. Zimmermann, "RETO, an Optimal Clocking Algorithm for Digital Synchronous Circuits", SFB-124, Report-No. 42/93, Universität Kaiserslautern, Fachbereich Informatik, 1993

[Hol75]   J. H. Holland, "Adaptation in Natural and Artificial Systems", University of Michigan Press, Ann Arbor, Michigan, 1975

[HoM87]   E. H. Horneber, W. Mathis, "A Closed-Form Expression for Signal Delay in CMOS-Driven Branched Transmission Lines", Proc. of the IFIP TC 10/WG 10.5 International Conference on Very Large Scale Integration, Vancouver, Canada, pp. 353-362, August 1987

[HoS98]   H. Hou, S. S. Sapatnekar, "Routing Tree Topology Construction to Meet Interconnect Timing Constraints", Proc. of the ACM Int. Symposium on Physical Design ISPD 98, pp. 205-210, 1998

[HSS91]   N. D. Holmes, N. A. Sherwani, M. Sarrafzadeh, "Algorithms for Three-Layer Over-the-Cell Channel Routing", Int. Conference On Computer-Aided Design ICCAD 91, pp. 428-431, 1991

[HwR92]   F. K. Hwang, D. S. Richards, "Steiner Tree Problems", Networks, Vol. 22, No. 1, pp. 55-89, 1992

[JaK89]   M. A. B. Jackson, E. S. Kuh, "Performance-Driven Placement of Cell Based ICs", Proc. of the 26th ACM/IEEE Design Automation Conference DAC, pp. 370-375, 1989

[Joh96]   F. M. Johannes, "Partitioning of VLSI Circuits and Systems", Proc. of the 33rd ACM/IEEE Design Automation Conference DAC, pp. 83-87, 1996

[JSK90]   M. A. B. Jackson, A. Srinivasan, E. S. Kuh, "A Fast Algorithm for Performance-Driven Placement", Proc. of the International Conference on Computer-Aided Design ICCAD 90, pp. 328-331, 1990

[KAK97]   G. Karypis, R. Aggarwal, V. Kumar, S. Shekhar, "Multilevel Hypergraph Partitioning: Application in VLSI Domain", Proc. of the 34th ACM/IEEE Design Automation Conference DAC, pp. 526-529, 1997

[KaR92]   A. B. Kahng, G. Robins, "A New Class of Iterative Steiner Tree Heuristics with Good Performance", IEEE Transactions on Computer-Aided Design, Vol. 11, No. 7, pp. 893-902, July 1992

[KeL70]   B. W. Kernighan, S. Lin, "An efficient heuristic procedure for partitioning graphs", Bell Syst. Technical Journal, Vol. 49, No. 2, pp. 291-307, Feb. 1970

[Kel89]   W. Keller, "Ein Modell zur entwurfsbegleitenden hierarchischen Behandlung des Zeitverhaltens beim physikalischen VLSI-Entwurf", Dissertation, Universität Kaiserslautern, Fachbereich Informatik, 1989

[KGV83]   S. Kirkpatrick, C. D. Gelatt, M. P. Vecchi, "Optimization by Simulated Annealing", Science, vol. 220, pp. 671-680, 1983

[KlB87]   R. Kling, P. Bannerjee, "ESP: A New Standard Cell Placement Package Using Simulated Evolution", Proc. of the 24th ACM/IEEE Design Automation Conference DAC, pp. 60-66, 1987

[KMB81]   L. T. Kou, G. Markowsky, L. Berman, "A fast algorithm for Steiner trees", Acta Informatica, Vol. 15, pp. 141-145, 1981

[KMM96]   A. B. Kahng, K. Masuko, S. Muddu, "Analytical Delay Models for VLSI Interconnects under Ramp Input", Proc. of the Int. Conference On Computer-Aided Design ICCAD 96, pp. 30-36, 1996

[KMO89]   R. Kolla, P. Molitor, H. G. Osthof, "Einführung in den VLSI-Entwurf", B. G. Teubner 1989

[Kri84]   B. Krishnamurthy, "An improved min-cut algorithm for partitioning VLSI networks", IEEE Transactions on Computers, Vol. C-33, pp. 438-446, May 1984

[KSJ91]   J. M. Kleinhans, G. Sigl, F. M. Johannes, K. J. Antreich, "GORDIAN: VLSI Placement by Quadratic Programming and Slicing Optimization", IEEE Transactions on Computer-Aided Design, Vol. 10, No. 3, pp. 356-365, January 1991

[KuP89]   F. J. Kurdahi, A. C. Parker, "Techniques for Area Estimation of VLSI Layouts", IEEE Transactions on Computer-Aided Design, Vol. 8, No. 1, pp. 81-92, January 1989

[Kur96]   S. Kurz, "Taktverdrahtung im Chip Planner des hierarchischen VLSI-Entwurfssystems PLAYOUT", Diplomarbeit, Fachbereich Informatik, Universität Kaiserslautern, 1996

[LaD86]   D. P. LaPotin, S. W. Director, "Mason: A Global Floorplanning Approach for VLSI Design", IEEE Transactions on Computer-Aided Design, Vol. CAD-5, No 4, pp. 477-489, January 1986

[LCL96]   J. Lillis, C.-K. Cheng, T.-T. Y. Lin, C.-Y. Ho, "New Performance Driven Routing Techniques With Explicit Area/Delay Tradeoff and Simultaneous Wire Sizing", Proc. of the 33rd ACM/IEEE Design Automation Conference DAC, pp. 395-400, 1996

[LCL95]   J. Lillis, C.-K. Cheng, T.-T. Y. Lin, "Optimal Wire Sizing and Buffer Insertion for Low Power and a Generalized Delay Model", Proc. of the Int. Conference On Computer-Aided Design ICCAD 95, pp. 138-143, 1995

[Len90]   T. Lengauer, "Combinatorial Algorithms for Integrated Circuit Layout", B. G. Teubner, Stuttgart, 1990

[Lic98]   J. Lichtermann, "Eine Architektur zur Echtzeitvisualisierung von Volumendaten", Dissertation, Universität Kaiserslautern, Fachbereich Informatik, 1998

[LLL96]   J. Li, J. Lillis, L.-T. Liu, C.-K. Cheng, "New Spectral Linear Placement and Clustering Approach", Proc. of the 33rd ACM/IEEE Design Automation Conference DAC, pp. 88-93, 1996

[LPH91]   M.-S. Lin, H.-W. Perng, C.-Y. Hwang, Y.-L. Lin, "Channel Density Reduction by Routing Over the Cells", Proc. of the 28th ACM/IEEE Design Automation Conference DAC, pp. 120-125, 1991

[LST87]   W. K. Luk, P. Sipala, M. Tamminen, D. Tang, L. S. Woo, C. K. Wong, "A Hierarchical Global Wiring Algorithm for Custom Chip Design", IEEE Transactions on Computer-Aided Design, Vol. CAD-6, No. 4, pp. 518-533, July 1987

[MaL89]   M. Marek-Sadowska, S. P. Lin, "Timing Driven Placement", Proc. of the International Conference on Computer-Aided Design ICCAD 89, pp. 94-97, 1989

[Mar93]   P. Marwedel, "Synthese und Simulation von VLSI-Systemen", C. Hanser Verlag, München, Wien, 1993

[Mar85]   P. Marwedel, "Ein Software-System zur Synthese von Rechnerstrukturen und zur Erzeugung von Mikrocode", Habilitationsschrift, Universität Kiel, 1985

[Mei91]   G. Meixner, "Global Routing of Very Large Scale Integrated Circuits based on Flow Methods and Timing Considerations", Dissertation, Universität Kaiserslautern, Fachbereich Informatik, 1991

[MMT87] M. Mogaki, C. Miura, H. Terai, "Algorithm for Block Placement with Size Optimization Technique by the Linear Programming Approach", Proc. of the International Conference On Computer-Aided Design ICCAD 87, pp. 80-83, 1987

[MPC90]   M. C. McFarland, A. C. Parker, R. Camposano, "The high-level Synthesis of Digital Systems", Proc. of the IEEE, Vol. 78, No. 2, pp. 301-318, February 1990

[Mul73]   H. Müller-Merbach. "Operations Research, Methoden und Modelle der Optimalplanung", Verlag F. Vahlen, München, 3. Auflage, 1973

[MSB94]   S. Madhwapathy, N. Sherwani, S. Bhingarde, A. Panyam, "A Unified Approach to Multilayer Over-the-Cell Routing", Proc. of the 31st ACM/IEEE Design Automation Conference DAC, pp. 182-187, 1994

[NBH89]   R. Nair, C. L. Berman, P. S. Hauge, E. J. Yoffa, "Generation of Performance Constraints for Layout", IEEE Transactions on Computer-Aided Design, Vol. 8, No 8, pp. 860-874, August 1989

[NLG95]   V. Narayananan, D. LaPotin, R. Gupta, G. Vijayan, "PEPPER - A Timing Driven Early Floorplanner", Proc. of the International Conference on Computer Design ICCD 95, pp. 230-235, 1995

[OkC96]   T. Okamoto, J. Cong, "Buffered Steiner Tree Construction with Wire Sizing for Interconnect Layout Optimization", Proc. of the Int. Conference On Computer-Aided Design ICCAD 96, pp. 44-49, 1996

[Ott83]   R. H. J. M. Otten, "Efficient Floorplan Optimization", Proc. of the International Conference on Computer Design: VLSI in Computers, ICCD'83, pp. 499-502, 1983

[Ott82]   R. H. J. M. Otten, "Automatic Floorplan Design", Proc. of the 19th ACM/IEEE Design Automation Conference DAC, pp. 261-267, 1982

[PaS89]   J. Paulokat, E. Siepmann, "Die Quadro-Partitionierung: Ein neues Partitionierungsverfahren für den Chip Planner des VLSI-Entwurfssystems PLAYOUT", SFB-124, Report-No. 27/89, Universität Kaiserslautern, Fachbereich Informatik, 1989

[PaZ90]   J. Paulokat, G. Zimmermann, "Floorplanning with In-Place Quadripartitioning", Proc. of the Int. Workshop on Layout Synthesis, Research Triangle Park, North Carolina, USA, May 1990

[PiR90]   L. T. Piller, R. A. Rohrer, "Asymptotic Waveform Evaluation for Timing Analysis", IEEE Transactions on Computer-Aided Design, Vol. 9, No. 4, pp. 352-366, April 1990

[Pop96]   U. Pöpperl, "Globale Verdrahtungsplanung auf Eckpunktgraphen im Floorplanner des PLAYOUT VLSI-Entwurfssystems", Diplomarbeit, Fachbereich Informatik, Universität Kaiserslautern, 1996

[PrK92]   S. Prasitjutrakul, W. J. Kubitz, "A Performance-Driven Global Router for Custom VLSI Chip Design", IEEE Transactions on Computer-Aided Design, Vol. 11, No. 8, pp. 1044-1051, August 1992

[PrK89]   S. Prasitjutrakul, W. J. Kubitz, "Path-Delay Constrained Floorplanning: A Mathematical Programming Approach for Initial Placement", Proc. of the 26th ACM/IEEE Design Automation Conference DAC, pp. 364-369, 1989

[PrL88]   B. T. Preas, M. J. Lorenzetti (Eds.), "Physical Design Automation of VLSI Systems", Menlo Park, The Benjamin/Cummings Publ. Company, 1988

[RDJ94]   B. M. Riess, K. Doll, F. M. Johannes, "Partitioning Very Large Circuits Using Analytical Placement Techniques", Proc. of the 31st ACM/IEEE Design Automation Conference DAC, pp. 646-651, 1994

[RKG92]   C. Ramachandran, F. J. Kurdahi, D. D. Gajski, A. C.-H. Wu, V. Chaiyakul, "Accurate Layout Area and Delay Modeling for System Level Design", Proc. of the International Conference on Computer-Aided Design ICCAD 92, pp. 355-361, 1992

[Sak83]   T. Sakurai, "Approximation of Wiring Delay in MOSFET LSI", IEEE Journal of Solid-State Circuits, Vol. sc-18, No. 4, pp. 418-426, 1983

[San89]   L. A. Sanchis, "Multiple-Way Network Partitioning", IEEE Transactions on Computers, Vol. 38, No. 1, pp. 62-81, January 1989

[Sap94]   S. S. Sapatnekar, "RC Interconnect Optimization under the Elmore Delay Model", Proc. of the 31st ACM/IEEE Design Automation Conference DAC, pp. 387-391, 1994

[SaW96]   M. Sarrafzadeh, C. K. Wong, "An Introduction to VLSI Physical Design", McGrawHill International Editions, 1996

[SaY95]   S. M. Sait, H. Youssef, "VLSI Physical Design Automation: Theory and Practice", McGraw-Hill, London, 1995

[SDJ91]   G. Sigl, K. Doll, F. M. Johannes, "Analytical Placement: A Linear or a Quadratic Objective Function?", Proc. of the 28th ACM/IEEE Design Automation Conference DAC, pp. 427-432, 1991

[SeS86]   C. Sechen, A. Sangiovanni-Vincentelli, "TimberWolf 3.2: A New Standard Cell Placement and Global Routing Package", Proc. of the 23rd ACM/IEEE Design Automation Conference DAC, pp. 432-439, 1986

[SeS85]   C. Sechen, A. Sangiovanni-Vincentelli, "The TimberWolf Placement and Routing Package", IEEE Journal of Solid-State Circuits, Vol. sc-20, No. 2, pp. 510-522, April 1985

[ShB87]   L. Sha, T. Blank, "ATLAS - A Technique for Layout using Analytic Shapes", Proc. of the International Conference On Computer-Aided Design ICCAD 87, pp. 84-87, 1987

[ShK87]   E. Shragowitz, S. Keel, "A Global Router Based on a Multicommodity Flow Model", INTEGRATION, the VLSI Journal, Vol. 5, pp. 3-16, 1987

[ShM91]   K. Shahookar, P. Mazumder, "VLSI Cell Placement Techniques", ACM Computing Surveys, Vol. 23, pp. 143-220, 1991

[Sie91]   E. Siepmann, "Entwurfstheorie und Entwurfsdatenmodellierung für CAD-Frameworks", Dissertation, Universität Kaiserslautern, Fachbereich Informatik, 1991

[Sol91]   M. Schölzke, "Zeitbehandlung beim Entwurf von hochintegrierten synchronen Digitalschaltungen während der Repartitionierungsphase des PLAYOUT-Systems", Diplomarbeit, Fachbereich Informatik, Universität Kaiserslautern, 1991

[SRP95]   D. Singh, J. Rabaey, M. Pedram, F. Catthoor, S. Rajgopal, N. Sehgal, T. Mozdzen, "Power-conscious CAD Tools and Methodologies: a Perspective", Proc. of the IEEE, Vol. 83, No. 4, pp. 570-594, April 1995

[SSL93]   S. Sutanthavibul, E. Shragowitz, R.-B. Lin, "An Adaptive Timing-Driven Placement for High Performance VLSI's", IEEE Transactions on Computer-Aided Design, Vol. CAD-12, No. 10, pp. 1488-1498, October 1993

[Sto83]   L. Stockmeyer, "Optimal Orientations of Cells in Slicing Floorplan Design", Information and Control, Vol. 57, pp. 91-101, 1983

[SuA95]   B. Schürmann, J. Altmeyer, "The Effect of Pin Constraints on Layout Ares", Proc. IEEE European Design and Test Conference (ED&TC), Paris, 1995

[SuK87]   P. R. Suaris, G. Kedem, "Quadrisection: A New Approach to Standard Cell Layout", Proc. of the International Conference on Computer-Aided Design ICCAD 87, pp. 474-477, 1987

[Sur97]   B. Schürmann, "ECAD-Entwurfsmanagement", Habilitationsschrift, Fachbereich Informatik, Universität Kaiserslautern, 1997

[Sur92]   B. Schürmann, "A 280000 Standard Cells Test Design - First Experiences with the PLAYOUT Top-Down Design System", Proc. of the Int. ACM/SIGDA Workshop on Layout Synthesis, pp. 93-104, Research Triangle Park, North Carolina, 1992

[Sur88]   B. Schürmann, "Hierarchisches Top Down Chip Planning", Informatik-Spektrum, Vol. 11, No. 2, pp. 57-70, 1988

[SuS93]   W.-J. Sun, C. Sechen, "Efficient and Effective Placement for Very Large Circuits", Proc. of the International Conference on Computer-Aided Design ICCAD 93, pp. 170-177, 1993

[SuS90]   S. Sutanthavibul, E. Shragowitz, "An Adaptive Timing-Driven Layout for High Speed VLSI", Proc. of the 27th ACM/IEEE Design Automation Conference DAC, pp. 90-95, 1990

[SuZ96]   B. Schürmann, G. Zimmermann, "PLAYOUT - A Hierarchical Layout System", akzeptiert als Kapitel des Buchs "VLSI Design Environments and Silicon Compilation", ABLEX, 1996

[SwK72]   D. G. Schweikert, B. W. Kernighan, "A Proper Model for the Partitioning of Electrical Circuits", Proc. of the 9th Design Automation Workshop, pp. 57-62, 1972

[SwS95]   W. Swartz, C. Sechen, "Timing Driven Placement for Large Standard Cell Circuits", Proc. of the 32nd ACM/IEEE Design Automation Conference DAC, pp. 211-215, 1995

[SwS90]   W. Swartz, C. Sechen, "New Algorithms for the Placement and Routing of Macro Cells", Proc. of the International Conference on Computer-Aided Design ICCAD 90, pp. 336-339, 1990

[TKH88]   R. S. Tsay, E. S. Kuh, C. P. Hsu, "PROUD: A Sea-Of-Gate Placement Algorithm", IEEE Design & Test of Computers, pp. 44-56, 1988

[Tsa93]   R.-S. Tsay, "An Exact Zero-Skew Clock Routing Algorithm", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 12, No. 2, pp. 242-249, February 1993

[UKH85]   K. Ueda, H. Kitazawa, I. Harada, "CHAMP: Chip Floor Plan for Hierarchical VLSI Layout Design", IEEE Transactions on Computer-Aided Design, Vol. CAD-4, No 1, pp. 12-22, January 1985

[VeK83]   M. P. Vecchi, S. Kirkpatrick, "Global Wiring by Simulated Annealing", IEEE Transactions on Computer-Aided Design, Vol. CAD-2, No. 4, pp. 215-222, October 1983

[Wag88]   K. D. Wagner, "Clock System Design", IEEE Design & Test of Computers, pp. 9-27, October 1988

[WaW92]   T.-C. Wang, D. F. Wong, "Optimal Floorplan Area Optimization", IEEE Transactions on Computer-Aided Design, Vol. 11, No. 8, pp. 992-1002, August 1992

[Win87]   P. Winter, "Steiner Problem in Networks: A Survey", Networks, Vol. 17, pp. 129-167, 1987

[WKC89]   S. Wimer, I. Koren, I. Cederbaum, "Optimal Aspect Ratios of Building Blocks in VLSI", IEEE Transactions on Computer-Aided Design, Vol. 8, No. 2, pp. 139-145, February 1989

[WoS89]   D. F. Wong, P. S. Sakhamuri, "Efficient Floorplan Area Optimization", Proc. of the 26th ACM/IEEE Design Automation Conference DAC, pp. 586-589, 1989

[XKW96]   T. Xue, E. S. Kuh, D. Wang, "Post Global Routing Crosstalk Risk Estimation and Reduction", Proc. of the Int. Conference On Computer-Aided Design ICCAD 96, pp. 302-309, 1996

[Zim90]   G. Zimmermann, "VLSI Area Estimation Tolerances - Shape Function Generation vs. Floorplanning", Proc. of the EURO ASIC '90, Paris, pp. 202-207, 1990

[Zim89]   G. Zimmermann, "PLAYOUT - A Hierarchical Design System", Information Processing '89, G. X. Ritter (ed.), Elsevier Science Publishers B.V. (North Holland), IFIP, pp. 905-910, 1989

[Zim88]   G. Zimmermann, "A New Area Shape Function Estimation Technique for VLSI Layouts", Proc. of the 25th ACM/IEEE Design Automation Conference DAC, pp. 60-65, 1988